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EXAMINER	
FLOURNOY, HORACE L	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,277	SPENCER, ANDREW M.	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.

- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-12 and 14-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-12 and 14-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/27/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action has been issued in response to amendment filed 7 April 2006. Claims 1-19 are pending. Applicant's arguments have been carefully and respectfully considered, but they are not entirely persuasive, as will be discussed in more detail below, even in light of the instant amendments. Accordingly, this action has been made FINAL.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

As required by **M.P.E.P.** 609(c), the applicant's submission of the Information Disclosure Statements dated **06/27/2003** is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P.** 609(c), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

Claim Rejections - 35 USC § 112

RCB 6/20/06

With respect to claims 1, 5, and 12, the examiner acknowledges the remarks on page 7 of the applicants response with regard to previous 35 USC § 112, second paragraph rejections of these claims. Accordingly the previous 35 USC § 112 rejections are herewith withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8, 10-12, and 14-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsunoda et al. (U.S. PG Pub. no. 2003/0028733, hereafter referred to as Tsunoda) with MPCD (Microsoft Computer Dictionary) offered as extrinsic evidence.

With respect to **independent claim 1**,

> *"An integrated memory device* **[Tsunoda discloses in FIG. 1, 101: "Memory Apparatus" and associated text]** *that comprises: a nonvolatile memory array;* **[Tsunoda discloses in FIG. 1, 102: "Flash Memory"]** *and a nonvolatile buffered memory interface* **[Tsunoda teaches this limitation in FIG. 1, element 113]** *integrated on a substrate with said nonvolatile memory array,* **[See paragraph [0124], lines 1-12]** *wherein the memory interface comprises: one or more volatile buffers* **[Tsunoda teaches this limitation in FIG. 1, element 103]** *configured to buffer data for read operations;* **[disclosed in paragraph [0110]. The examiner interprets this limitation as a volatile buffer that is used for read operations or as data. Tsunoda discloses in paragraph [0110], "The**

read sector data (SCTn) is transferred...from the data buffer 108 through the SDRAM-buffer transfer circuit 607 and the MUX/DEMUX 0 (609) to the SDRAM interface control circuit 107, and written in the SDRAM 103." Tsunoda teaches a volatile buffer (SDRAM-buffer) configured to buffer data (transfer) for read operations (read data).] *and a table memory* **[disclosed in paragraphs [0105] and [0107]]** *configured to indicate one or more addresses within the nonvolatile memory array that have been recently accessed. ~~associated with data buffered in the one or more volatile buffers.~~"* **[Tsunoda teaches this limitation, e.g. in paragraph [0130] "An updating number of times 1705 records how many times data on the SDRAM 103 is updated by the host 111 after the data is transferred from the flash memory 102 to the SDRAM 103. "]**

With respect to **independent claim 7 (and claim 19)**,

"An integrated memory device **[Tsunoda discloses in FIG. 1, 101: "Memory Apparatus" and associated text]** *that comprises: a nonvolatile memory array* **[Tsunoda discloses in FIG. 1, 102: "Flash Memory"]***: and a nonvolatile buffered memory interface* **[Tsunoda teaches this limitation in FIG. 1, element 113]** *integrated on a substrate with said nonvolatile memory array,* **[See paragraph [0124], lines 1-12]** *wherein the memory interface comprises: one or more volatile buffers* **[Tsunoda teaches this limitation in FIG. 1, element 103]** *configured to buffer data for read operations;* **[disclosed in paragraph [0110]. The examiner interprets this limitation as a volatile buffer that is used for read operations or as data. Tsunoda discloses in paragraph [0110], "The**

read sector data (SCTn) is transferred...from the data buffer 108 through the SDRAM-buffer transfer circuit 607 and the MUX/DEMUX 0 (609) to the SDRAM interface control circuit 107, and written in the SDRAM 103." Tsunoda teaches a volatile buffer (SDRAM-buffer) configured to buffer data (transfer) for read operations (read data).] *and a table memory configured to indicate one or more addresses associated with data buffered in the one or more volatile buffers;* **[disclosed in paragraphs [0105] and [0107]]** ~~*The device of claim 1,*~~ *wherein the memory interface further comprises: an interface control module that is configured to receive read commands specifying a memory address,* **[Tsunoda discloses this limitation, e.g. in FIG. 1, element 107: "SDRAM I/F Control Circuit" and associated text]** *wherein the interface control module is coupled to the memory array* **[See FIG. 1]** *to conduct read operations to satisfy the read commands and to prepare read buffers to satisfy anticipated read commands."* **[this limitation is disclosed, e.g. in paragraph [0064].]**

With respect to **independent claim 10 (and claim 17),**

"A method of providing access to stored data, the method comprising: preserving during an absence of electrical power information indicative of data in one or more read buffers; **[Tsunoda discloses in paragraphs [0046] and [0047], "By the storage function, the data transferred to the flash memory 4020 can be held on the flash memory 4020 even if it is lost from the SDRAM 4010 because of a stop of the power supply to the memory apparatus 4000...The storage function is executed when an operation status of the memory**

apparatus 4000 satisfies predetermined storage execution conditions. One of the storage execution conditions is, for example a stop of the power supply."] *and restoring the data to the one or more read buffers when power returns;* **[disclosed, e.g. in paragraph [0049], lines 3-4]** ~~*The method of claim 9, wherein said preserving comprises: detecting a pending power-down;*~~ **[See FIG. 3, element 311, and all associated text within specification]** *for each of the one or more read buffers, storing in nonvolatile memory a starting address* **[See FIG. 3, element 307, and all associated text within specification]** *of memory blocks that have been recently accessed.* ~~*associated with data in the read buffer."*~~ **[Tsunoda teaches this limitation, e.g. in paragraph [0130] "An updating number of times 1705 records how many times data on the SDRAM 103 is updated by the host 111 after the data is transferred from the flash memory 102 to the SDRAM 103. "]**

With respect to **independent claim 14 (and claim 11),**

A method of providing access to stored data, the method comprising: preserving during an absence of electrical power information indicative of data in one or more read buffers; **[Tsunoda discloses in paragraphs [0046] and [0047], "By the storage function, the data transferred to the flash memory 4020 can be held on the flash memory 4020 even if it is lost from the SDRAM 4010 because of a stop of the power supply to the memory apparatus 4000...The storage function is executed when an operation status of the memory apparatus 4000 satisfies predetermined storage execution conditions. One of the storage execution conditions is, for example a stop of the power**

supply."] *when power returns, determining whether a restore operation is enabled;* **[disclosed, e.g. in paragraph [0049], lines 3-4]** *and if the restore operation is enabled, restoring the data to the one or more read buffers when power returns* **[disclosed, e.g. in paragraph [0049], lines 3-4]** ~~*The method of claim 13*~~*, wherein the one or more read buffers are integrated on a substrate with a nonvolatile memory array, and wherein said restoring comprises for each of the one or more read buffers: retrieving a start address from the nonvolatile memory wherein the start address represents an address that has been recently accessed ; and filling the read buffer with data retrieved from the nonvolatile memory array starting at the start address."* **[Tsunoda teaches this limitation, e.g. in paragraph [0130] "An updating number of times 1705 records how many times data on the SDRAM 103 is updated by the host 111 after the data is transferred from the flash memory 102 to the SDRAM 103. "]**

With respect to **independent claim 15**,

"A digital device that comprises: a memory having a ~~*nonvolatile*~~ *buffered memory interface with one or more read buffers and a processor coupled to the memory device* **[Tsunoda discloses this limitation, e.g. in FIG. 1, element 111: "Host" and associated text within specification. Tsunoda further discloses in paragraph [0040], "...the host 4040 is an information processor such as a CPU or ASIC incorporated in the information terminal. In the memory apparatus 4000, operation programs for, for example, enabling the host 4040 to execute various information processing, can be stored."]** *and configured to retrieve stored information from the memory* **[disclosed in**

paragraphs [0004], [0005], [0040] and FIG. 1 elements 111 and 112.] *wherein the processor causes the memory to receive a power down command before electrical power is removed from the memory,* **[See FIG. 3, element 311, and all associated text within specification]** *and wherein the buffered memory interface* **[Tsunoda discloses this limitation, e.g. in FIG. 1, element 107: "SDRAM I/F Control Circuit" and associated text]** *responsively stores in a nonvolatile memory information that represents one or more addresses within the memory that have been recently accessed ~~indicative of data in said one or more read buffers.~~"* **[Tsunoda teaches this limitation, e.g. in paragraph [0130] "An updating number of times 1705 records how many times data on the SDRAM 103 is updated by the host 111 after the data is transferred from the flash memory 102 to the SDRAM 103. " This limitation is further disclosed e.g. in paragraphs [0046] and [0047]]**

With respect to **claim 2**,

"The device of claim 1, wherein the table memory is volatile, and wherein the memory interface is configured to preserve contents of the table memory in nonvolatile memory during absences of electrical power" **is disclosed in paragraph [0112]. [Tsunoda discloses in paragraph [0112], "by transferring the data on the SDRAM 103 to the flash memory 102, the data can be held even after the power is turned off.]**

With respect to **claim 3**,

"The device of claim 2, wherein the memory interface is further configured to restore the contents of table memory from the nonvolatile memory when electrical power returns" **[Tsunoda discloses in paragraphs [0098] and [0099], "Since the SDRAM 103 is a volatile memory, the information stored in the nonvolatile area 204 on the SDRAM 103 is copied to the flash memory 102 before the power is turned OFF, and held on the flash memory 102... [0099] Use of the foregoing address space on the SDRAM 103 enables the following processing to be executed. After the power is turned ON, program data on the flash memory 102 is copied to the volatile area 203 of the SDRAM 102, and the host 111 can use the program by accessing the volatile area 203 on the SDRAM 103."]**

With respect to **claim 4**,

"The device of claim 1, wherein when electrical power returns, the memory interface is further configured to restore the one or more volatile buffers to a state preceding the absence of electrical power" **[Tsunoda discloses in paragraphs [0098] and [0099], "Since the SDRAM 103 is a volatile memory, the information stored in the nonvolatile area 204 on the SDRAM 103 is copied to the flash memory 102 before the power is turned OFF, and held on the flash memory 102... [0099] Use of the foregoing address space on the SDRAM 103 enables the following processing to be executed. After the power is turned ON, program data on the flash memory 102 is copied to the**

volatile area 203 of the SDRAM 102, and the host 111 can use the program by accessing the volatile area 203 on the SDRAM 103."]

With respect to **claims 5 (and claim 18)**,

"The device of claim 1, wherein the one or more volatile buffers comprise: a plurality of read buffers each associated with a different region of the memory array and configured to buffer only data for read operations on an associated region" **[Tsunoda discloses in paragraph [0107], "The mapping table 603 is for allocating the nonvolatile area 204 on the address space in the SDRAM 103 to the logical sector address 205 of the flash memory 102. The ADRf1 generation circuit 604 generates a logical sector address on the flash memory 102. ... In reading, data of the SDRAM 103 sent from the SDRAM interface control circuit 107 is sent to the data bus of the SDRAM interface 112 connected to the host, or the SDRAM-buffer transfer circuit 607."]**

With respect to **claim 6**,

"The device of claim 1, wherein the memory array comprises magnetic random access memory (MRAM) cells" **[Tsunoda discloses in paragraph [0124], "Further, types of the nonvolatile memory and the volatile memory of the present invention are not limited to the flash memory 102 or the SDRAM 103. For example, regarding the nonvolatile memory, similar processing can be carried out in a ferroelectric memory or an MRAM (magnetic memory)."]**

With respect to **claims 8 (and 19)**,

"The device of claim 7, further comprising: an error correction code (ECC) decoder **[See paragraph [0097] and FIG. 1 element 109]** *coupled between the memory array* **[FIG.1, element 102]** *and the one or more volatile buffers"* **[FIG. 1, element 103.]**

With respect to **claim 12**,

"The method of claim 10, wherein before said detecting the method further comprises: receiving a read command that comprises a read address **[Tsunoda discloses in paragraph [0052], "The memory apparatus 4000 includes a function for enabling the host 4040 to designate changing of the address correspondence setting information. The memory apparatus 4000 includes a function of saving the address correspondence setting information in the flash memory 4020. The memory apparatus 4000 includes a function of reading the address correspondence setting information from the flash memory 4020."]** *determining whether data from the read address is buffered in a read buffer* **[disclosed in paragraphs [0050] and [0051]]** *retrieving data from a location in a memory array associated with the read address if the data is not buffered and responding to the read command with data from said one of the plurality of read buffers if the data is buffered"*

With respect to **claim 16**,

"The device of claim 15, wherein the memory interface is further configured to reload the one or more read buffers with data in accordance with information from the nonvolatile memory when power returns" **[disclosed, e.g. in paragraph**

[0049], lines 3-4. Tsunoda further discloses in paragraphs [0098] and [0099], "Since the SDRAM 103 is a volatile memory, the information stored in the nonvolatile area 204 on the SDRAM 103 is copied to the flash memory 102 before the power is turned OFF, and held on the flash memory 102... [0099] Use of the foregoing address space on the SDRAM 103 enables the following processing to be executed. After the power is turned ON, program data on the flash memory 102 is copied to the volatile area 203 of the SDRAM 102, and the host 111 can use the program by accessing the volatile area 203 on the SDRAM 103."]

ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

Applicant's arguments filed **April 7, 2006** have been fully considered but they are not deemed to be persuasive and, as required by **M.P.E.P. 707.07(f)**, a response to these arguments appears below.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

POINT OF ARGUMENT for Claim 1:

With respect to the arguments on page 8, paragraph 1 of the applicant's remarks, the examiner believes that Tsunoda teaches *"a table memory configured to indicate one or more addresses within the nonvolatile memory array that have been recently accessed."* Tsunoda

teaches this limitation, e.g. in paragraph [0130] "An updating number of times 1705 records how many times data on the SDRAM 103 is updated by the host 111 after the data is transferred from the flash memory 102 to the SDRAM 103. " The examiner believes that these two limitations are analogous.

With respect to the arguments on page 8, paragraph 2 of the applicant's remarks, the examiner believes that Tsunoda teaches clearly in paragraph [0124] "*a nonvolatile buffered memory interface integrated on a substrate with said nonvolatile memory array*". The examiner apologizes for any confusion, but Tsunoda, as interpreted by the examiner, anticipates the applicant's claim in memory apparatus 101, e.g.

POINT OF ARGUMENT for Claim 7:

With respect to the argument on page 9, paragraph 1 of the applicant's remarks, the examiner believes that Tsunoda teaches *wherein the interface control module is coupled to the memory array* **[See FIG. 1]** *to conduct read operations to satisfy the read commands and to prepare read buffers to satisfy anticipated read commands."* **This limitation is disclosed, e.g. in paragraph [0064].** Therefore, the examiner respectfully disagrees with the applicant's argument.

With respect to the argument on page 9, paragraph 2 of the applicant's remarks, the examiner apologizes for any misinterpretation of claim limitations. See the rejection of claim 7 above for corrections.

POINT OF ARGUMENT for Claim 10:

With respect to the arguments to claim 10 of the applicant's remarks, the examiner believes that Tsunoda teaches *"a table memory configured to indicate one or more addresses within the nonvolatile memory array that have been recently accessed."* Tsunoda teaches this limitation, e.g. in paragraph [0130] "An updating number of times 1705 records how many times data on the SDRAM 103 is updated by the host 111 after the data is transferred from the flash memory 102 to the SDRAM 103. " The examiner believes that these two limitations are analogous.

POINT OF ARGUMENT for Claim 14:

With respect to the arguments to claim 14 of the applicant's remarks, the examiner believes that Tsunoda teaches *"a table memory configured to indicate one or more addresses within the nonvolatile memory array that have been recently accessed."* Tsunoda teaches this limitation, e.g. in paragraph [0130] "An updating number of times 1705 records how many times data on the SDRAM 103 is updated by the host

111 after the data is transferred from the flash memory 102 to the SDRAM 103. " The examiner believes that these two limitations are analogous.

POINT OF ARGUMENT for Claim 15:

With respect to the arguments to claim 15 of the applicant's remarks, the examiner believes that Tsunoda teaches *"a table memory configured to indicate one or more addresses within the nonvolatile memory array that have been recently accessed."* Tsunoda teaches this limitation, e.g. in paragraph [0130] "An updating number of times 1705 records how many times data on the SDRAM 103 is updated by the host 111 after the data is transferred from the flash memory 102 to the SDRAM 103. " The examiner believes that these two limitations are analogous.

CONCLUSION

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Horace L. Flourney
Patent Examiner
Art unit: 2189

Reginald G. Bragdon
Supervisory Patent Examiner
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